

## 1. General description

---

PTN3460 is an (embedded) DisplayPort to LVDS bridge that enables connectivity between an (embedded) DisplayPort (eDP) source and LVDS display panel. It processes the incoming DisplayPort (DP) stream, performs DP to LVDS protocol conversion and transmits processed stream in LVDS format.

PTN3460 provides significant flexibility to optimally fit under different platform environments with programmability of its internal functions. PTN3460 is powered by 3.3 V and/or 1.8 V supplies and is available in the HVQFN56 7 mm × 7 mm package with 0.4 mm pitch.

## 2. Features and benefits

---

- Supports DP Main Link operation with 1 or 2 lanes
- Supports DP Main Link rate—Reduced Bit Rate (1.62 Gbit/s) and High Bit Rate (2.7 Gbit/s)
- Supports downspreading on DP Link to reduce EMI
- Supports Full Link training and Fast Link training
- Supports eDP authentication options—ASSR, alternate framing
- Supports LVDS single and dual bus operation
- Supports LVDS color depths—18 bpp, 24 bpp
- Supports LVDS pixel clock up to 112 MHz
- Supports 1920 × 1200 at 60 Hz resolution in LVDS Dual-bus mode
- Supports center spreading of LVDS clock to reduce EMI
- Supports panel power up/down control
- Supports device configurability via pins, DP AUX, I<sup>2</sup>C
- eDP complying PWM generator
- Supports EDID ROM emulation
- No external timing reference
- Supports power management modes in tune with platform needs
- Power supply: (3.3 V ± 10 %) or (3.3 V ± 10 % and 1.8 V ± 5 %)
- ESD: 6 kV HBM
- Commercial operating temperature range: 0 °C to 70 °C
- HVQFN56 package 7 mm × 7 mm, 0.4 mm pitch; exposed center pad for thermal relief and electrical ground

## 3. Applications

---

- AIO platforms
- Netbooks/nettops
- Netbook platforms



Table 1. Ordering information

Type number	Package		Version
	Name	Description	
PTN3460BS	HVQFN56	plastic thermal enhanced very thin quad flat package; no leads; 56 terminals; body 7 × 7 × 0.85 mm <sup>[1]</sup> , 0.4 mm pitch	SOT949-2

[1] Maximum package height is 1 mm.

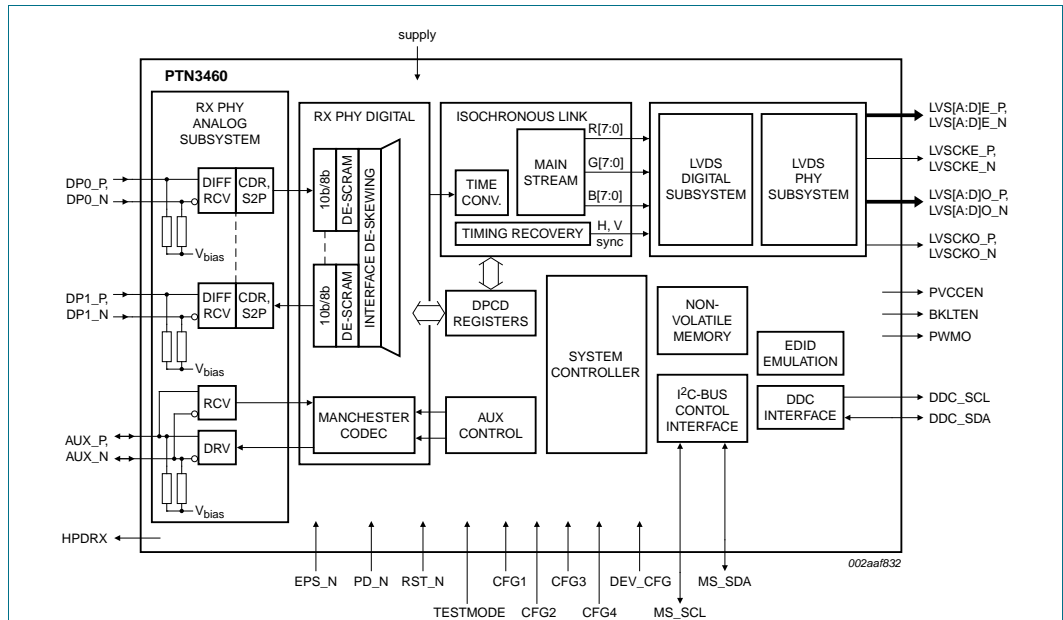


Fig 1. Block diagram of PTN3460

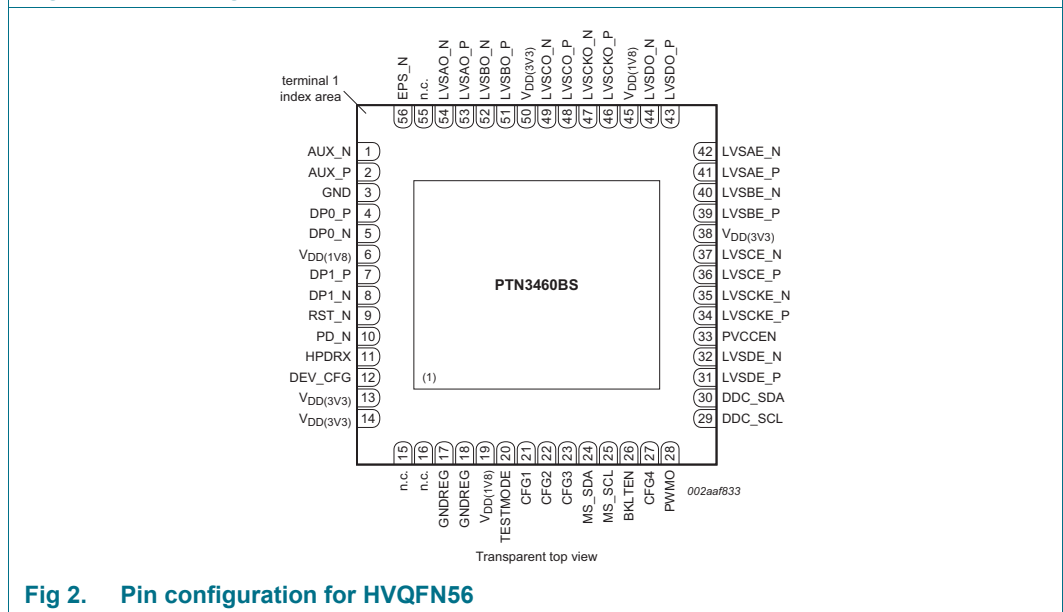


Fig 2. Pin configuration for HVQFN56

HVQFN56 : plastic thermal enhanced very thin quad flat package, no leads.  
56 terminals, body 7 x 7 x 0.85 mm

SOT949-2

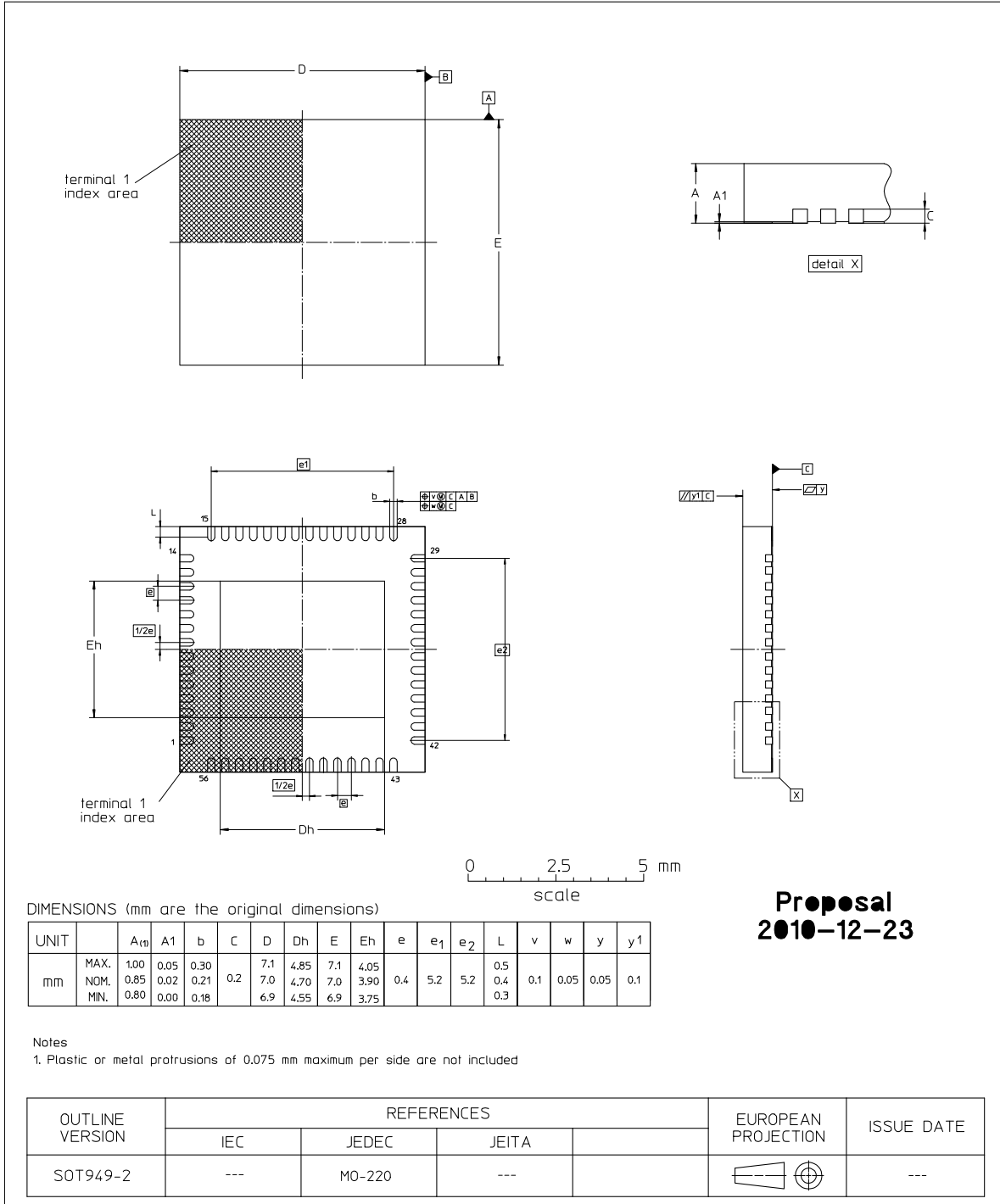


Fig 3. Package outline SOT949-2 (HVQFN56)

© NXP B.V. 2011.

All rights reserved.

For more information, please visit: <http://www.nxp.com>  
For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

Date of release: 2 June 2011  
Document identifier: PTN3460