

ES_LPC1756

Errata sheet LPC1756

Rev. 02 — 16 March 2010

Errata sheet

Document information

Info	Content
Keywords	LPC1756 errata
Abstract	<p>This errata sheet describes both the known functional problems and any deviations from the electrical specifications known at the release date of this document.</p> <p>Each deviation is assigned a number and its history is tracked in a table at the end of the document.</p>



Revision history

Rev	Date	Description
02	20100316	<ul style="list-style-type: none">The format of this errata sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.Added I2S.1 and Ethernet.1
01	20091014	<ul style="list-style-type: none">Added MCPWM.1

Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

1. Product identification

The LPC1756 devices typically have the following top-side marking:

```
LPC1756xxx
xxxxxxx
xxYYWWR[x]
```

The last/second to last letter in the third line (field 'R') will identify the device revision. This Errata Sheet covers the following revisions of the LPC1756:

Table 1. Device revision table

Revision identifier (R)	Revision description
'0'	Initial device revision

Field 'YY' states the year the device was manufactured. Field 'WW' states the week the device was manufactured during that year.

2. Errata overview

Table 2. Functional problems table

Functional problems	Short description	Revision identifier
I2S.1	XY divider will not work for PCLK-I2S higher than 74 MHz	'0'
Ethernet.1	Ethernet TxConsumeIndex register does not update correctly after the first frame is sent	'0'
PLL0.1	PLL0 (Main PLL) remains enabled and connected in Deep Sleep and Power-down modes	'0'
PCLKSELx.1	Peripheral Clock Selection Registers must be set before enabling and connecting PLL0	'0'
MCPWM.1	Input pins (MCI0-2) on the Motor Control PWM peripheral are not functional	'0'

Table 3. AC/DC deviations table

AC/DC deviations	Short description	Revision identifier
n/a	n/a	n/a

3. Functional problems detail

3.1 I2S.1: The XY divider (8-bit Fractional Rate Divider) will not work for PCLK_I2S (Peripheral clock for I2S) higher than 74 MHz

Introduction:

The transmitter/receiver MCLK (Master clock output) rate is generated using a fractional rate generator, dividing down the frequency of PCLK_I2S. Values of the numerator (X) and the denominator (Y) must be chosen to produce a frequency twice that desired for the receiver MCLK, which must be an integer multiple of the receiver bit clock rate.

Problem:

The XY divider (8-bit Fractional Rate Divider) will not work for PCLK_I2S (Peripheral clock for I2S) higher than 74 MHz.

Work-around:

Do not use PCLK_I2S signal higher than 74 MHz.

3.2 Ethernet.1: Ethernet TxConsumeIndex register does not update correctly after the first frame is sent

Introduction:

The transmit consume index register defines the descriptor that is going to be transmitted next by the hardware transmit process. After a frame has been transmitted hardware increments the index, wrapping the value to 0 once the value of TxDescriptorNumber has been reached. If the TxConsumeIndex equals TxProduceIndex the descriptor array is empty and the transmit channel will stop transmitting until software produces new descriptors.

Problem:

The TxConsumeIndex register is not updated correctly (from 0 to 1) after the first frame is sent. After the next frame sent, the TxConsumeIndex register is updated by two (from 0 to 2). This only happens the very first time, so subsequent updates are correct (even those from 0 to 1, after wrapping the value to 0 once the value of TxDescriptorNumber has been reached)

Work-around:

Software can correct this situation in many ways; for example, sending a dummy frame after initialization.

3.3 PLL0.1: PLL0 (Main PLL) remains enabled and connected in Deep Sleep and Power-down modes

Introduction:

If the main PLL (PLL0) is enabled and connected before entering Deep Sleep or Power-down modes, main PLL (PLL0) automatically turns off and disconnects after the chip enters Deep Sleep mode or Power-down mode leading to reduced power consumption.

Problem:

If the main PLL (PLL0) is enabled and connected before entering Deep Sleep or Power-down modes, it will remain enabled and connected after the chip enters Deep Sleep mode or Power-down mode causing the power consumption to be higher.

Work-around:

In the software, user must disable and disconnect the main PLL (PLL0) before entering Deep Sleep and Power-down modes to reduce the power consumption. This must be done only if the main PLL (PLL0) was enabled and connected before entering Deep Sleep mode or Power-down mode.

The code below demonstrates the steps to disable and disconnect the main PLL0:

```

PLL0CON &= ~(1<<1);           /* Disconnect the main PLL (PLL0) */

PLL0FEED = 0xAA;             /* Feed */

PLL0FEED = 0x55;            /* Feed */

while ((PLL0STAT & (1<<25)) != 0x00); /* Wait for main PLL (PLL0) to disconnect */

PLL0CON &= ~(1<<0);           /* Turn off the main PLL (PLL0) */

PLL0FEED = 0xAA;             /* Feed */

PLL0FEED = 0x55;            /* Feed */

while ((PLL0STAT & (1<<24)) != 0x00); /* Wait for main PLL (PLL0) to shut down */

/***** Then enter into Deep sleep mode or Power-down mode*****/

```

3.4 PCLKSELx.1: Peripheral Clock Selection Registers must be set before enabling and connecting PLL0

Introduction:

A pair of bits in the Peripheral Clock Registers (PCLKSEL0 and PCLKSEL1) controls the rate of the clock signal that will be supplied to APB0 and APB1 peripherals.

Problem:

If the Peripheral Clock Registers (PCLKSEL0 and PCLKSEL1) are set or changed after PLL0 is enabled and connected, the value written into the Peripheral Clock Selection Registers may not take effect. It is not possible to change the Peripheral Clock Selection settings once PLL0 is enabled and connected.

Work-around:

Peripheral Clock Selection Registers must be set before enabling and connecting PLL0.

3.5 MCPWM.1: Input pins (MCI0-2) on the Motor Control PWM peripheral are not functional

Introduction:

On the LPC1756, the Motor Control PWM (MCPWM) peripheral is optimized for three-phase AC and DC motor control applications and can also be used in applications which require timing, counting, capture, and comparison. The MCPWM contains three input pins (MCI0-2) for PWM channels 0, 1, and 2. The inputs can be used as feedbacks for controlling brushless DC motors with Hall sensors, and also can be used to trigger a Timer/Counter's (TC) capture or increment a channel's TC when MCPWM is configured as a timer/counter.

Problem:

The input pins (MCI0-2) are not functional.

Work-around:

The GPIO interrupts on port 0 or port 2 can be used instead of the MCPWM MCI0-2 pins. The GPIO interrupts give the ability to trigger an interrupt on both the rising and falling edge; therefore, all six states of the connected hall sensor can be detected through an interrupt.

4. AC/DC deviations detail

4.1 n/a

5. Legal information

5.1 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

5.2 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on a weakness or default in the customer application/use or the application/use of customer's third party customer(s) (hereinafter both referred to as "Application"). It is customer's sole responsibility to check whether the NXP Semiconductors product is suitable and fit for the Application planned. Customer has to do all necessary testing for the Application in order to avoid a default of the Application and the product. NXP Semiconductors does not accept any liability in this respect.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

5.3 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

6. Contents

1 **Product identification** 3

2 **Errata overview** 3

3 **Functional problems detail** 4

3.1 I2S.1: The XY divider (8-bit Fractional Rate Divider) will not work for PCLK_I2S (Peripheral clock for I2S) higher than 74 MHz 4

 Introduction:4

 Problem:4

 Work-around:4

3.2 Ethernet.1: Ethernet TxConsumeIndex register does not update correctly after the first frame is sent 4

 Introduction:4

 Problem:4

 Work-around:4

3.3 PLL0.1: PLL0 (Main PLL) remains enabled and connected in Deep Sleep and Power-down modes 5

 Introduction:5

 Problem:5

 Work-around:5

3.4 PCLKSELx.1: Peripheral Clock Selection Registers must be set before enabling and connecting PLL0 6

 Introduction:6

 Problem:6

 Work-around:6

3.5 MCPWM.1: Input pins (MCI0-2) on the Motor Control PWM peripheral are not functional. 6

 Introduction:6

 Problem:6

 Work-around:6

4 **AC/DC deviations detail** 6

4.1 n/a 6

5 **Legal information** 7

5.1 Definitions 7

5.2 Disclaimers 7

5.3 Trademarks 7

6 **Contents** 8

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2010.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 16 March 2010

Document identifier: ES_LPC1756_2