

ERRATA SHEET

Date: February 9, 2009
Document Release: Version 1.3
Device Affected: LPC2132/01

This errata sheet describes both the functional problems and any deviations from the electrical specifications known at the release date of this document.

Each deviation is assigned a number and its history is tracked in a table at the end of the document.

2009 Feb 09

Document revision history

Rev	Date	Description
1.3	February 9, 2009	1. Added Rev E
1.2	June 7, 2008	1. Added WDT.1 2. Added Table for Errata Notes 3. Added Errata Note 2
1.1	June 8, 2007	1. Added MAM.1 2. Added ESD.1
1.0	August 30, 2006	First version

Identification:

The LPC2132/01 devices typically have the following top-side marking:

LPC2132xxx
/01
xxxxxxx
xxYYWW R

The last letter in the last line (field 'R') will identify the device revision. This Errata Sheet covers the following revisions of the LPC2132/01:

Revision Identifier (R)	Comment
'D'	First device revision
'E'	Second device revision

Field 'YY' states the year the device was manufactured. Field 'WW' states the week the device was manufactured during that year.

Errata Overview - Functional Problems

Functional Problem	Short Description	Device Revision the problem occurs in
Core.1	Incorrect update of the Abort link register	D, E
Timer.1	Timer Counter reset occurs on incorrect edge in counter mode	D
SSP.1	Initial data bits/clocks corrupted in SSP transmission	D, E
MAM.1	Code execution failure can occur with MAM Mode 2	D
WDT.1	Accessing non-Watchdog APB registers in the middle of the feed sequence causes a reset	D

Errata Overview - AC/DC Deviations

AC/DC Deviations	Short Description	Device Revision the deviation occurs in
ESD.1	ESD weakness on RTCX1 pin	D

Errata Notes

Notes	Short Description	Device Revision the note applies to
Note 1	Port pin P0.31 must not be driven low during reset.	D, E
Note 2	When the input voltage is $V_i \geq V_{dd} I/O + 0.5 \text{ v}$ on port pin P0.25 (configured as general purpose input pin), current must be limited to less than 4 mA by using a series limiting resistor.	D, E

Functional Problems of LPC2132/01

Core.1 Incorrect update of the Abort Link register in Thumb state

Introduction: If the processor is in Thumb state and executing the code sequence STR, STMIA or PUSH followed by a PC relative load, and the STR, STMIA or PUSH is aborted, the PC is saved to the abort link register.

Problem: In this situation the PC is saved to the abort link register in word resolution, instead of half-word resolution.

Conditions:

The processor must be in Thumb state, and the following sequence must occur:

<any instruction>

<STR, STMIA, PUSH> <---- data abort on this instruction

LDR rn, [pc,#offset]

In this case the PC is saved to the link register R14_abt in only word resolution, not half-word resolution. The effect is that the link register holds an address that could be #2 less than it should be, so any abort handler could return to one instruction earlier than intended.

Work around: In a system that does not use Thumb state, there will be no problem.

In a system that uses Thumb state but does not use data aborts, or does not try to use data aborts in a recoverable manner, there will be no problem.

Otherwise the workaround is to ensure that a STR, STMIA or PUSH cannot precede a PC-relative load. One method for this is to add a NOP before any PC-relative load instruction. However this is would have to be done manually.

Timer.1 In counter mode, the Timer Counter reset does not occur on the correct incoming edge

Introduction: Timer0 and Timer1 can be used in a counter mode. In this mode, the Timer Counter register can be incremented on rising, falling or both edges which occur on a selected CAP input pin.

This counter mode can be combined with the match functionality to provide additional features. One of the features would be to reset the Timer Counter register on a match. The same would also apply for Timer1.

Problem The Timer Counter reset does not trigger on the same incoming edge when the match takes place between the corresponding Match register and the Timer Counter register. The Timer Counter register will be reset only on the next incoming edge.

Work-around: There are two possible workarounds:

1. Combine the Timer Counter reset feature with the "interrupt on match" feature. The interrupt on match occurs on the correct incoming edge. In the ISR, the Timer Counter register can also be reset. This solution can only work if no edges are expected during the duration of the ISR.

2. In this solution, the "interrupt on match" feature is not used. Instead, the following specific initialization can achieve the counting operation:

- a. Initialize the Timer Counter register to 0xFFFFFFFF.

- b. If "n" edges have to be counted then initialize the corresponding Match register with value n-1. For instance, if 2 edges need to be counted then load the Match register with value 1

More details on the above example:

- a. Edge 1- Timer overflows and Timer Counter (TC) is set to 0.
- b. Edge 2- TC=1. Match takes place.
- c. Edge 3- TC=0.
- d. Edge 4- TC=1. Match takes place.
- e. Edge 5- TC=0.

SSP.1 Initial data bits/clocks of the SSP transmission are shorter than subsequent pulses at higher frequencies

Introduction: The SSP is a Synchronous Serial Port (SSP) controller capable of operation on a SPI, 4-wire SSI or a Microwire bus. The SSP can operate at a maximum speed of 30MHz and it referred to as SPI1 in the device documentation.

Problem: At high SSP frequencies, it is found that the first four pulses are shorter than the subsequent pulses. At 30MHz, the first pulse can be expected to be approximately 10ns shorter and the second pulse around 5ns shorter. The remaining two pulses are around 2ns shorter than subsequent pulses. At 25MHz, the length of the first pulse would be around 7ns shorter. The subsequent three pulses are around 2ns shorter. At 20MHz only the first pulse is affected and it is around 2ns shorter. All subsequent pulses are fine. The deviation of the initial data bits/clocks will decrease as the SSP frequency decreases.

Work-around: None.

MAM.1 Under certain conditions in MAM Mode 2 code execution out of internal Flash can fail

Introduction: The MAM block maximizes the performance of the ARM processor when it is running code in Flash memory. It includes three 128-bit buffers called the Prefetch Buffer, the Branch Trail Buffer and the data buffer. It can operate in 3 modes; Mode 0 (MAM off), Mode 1 (MAM partially enabled) and Mode 2 (MAM fully enabled).

Problem: Under certain conditions when the MAM is fully enabled (Mode 2) code execution from internal Flash can fail. The conditions under which the problem can occur is dependent on the code itself along with its positioning within the Flash memory.

Workaround: If the above problem is encountered then Mode 2 should not be used. Instead, partially enable the MAM using Mode 1.

WDT.1: Accessing non-Watchdog APB registers during the feed sequence causes a reset.

Introduction: The Watchdog timer can reset the microcontroller within a reasonable amount of time if it enters an erroneous state.

Problem: After writing 0xAA to WDFEED, any APB register access other than writing 0x55 to WDFEED may cause an immediate reset.

Workaround: Avoid APB accesses in the middle of the feed sequence. This implies that interrupts and the GPDMA should be disabled while feeding the Watchdog.

AC/DC Deviations of the LPC2132/01**ESD.1: The LPC2132/01 does not meet the 2kV ESD requirements on the RTCX1 pin**

Introduction: The LPC2132/01 is rated for 2kV ESD. The RTCX1 pin is the input pin for the RTC oscillator circuit.

Problem: The LPC2132/01 does not meet the required 2kV ESD specified.

Workarounds: Observe proper ESD handling precautions for the RTCX1 pin.

Errata Notes

- Note 1:** Port pin P0.31 must not be driven low during reset. If low on reset the device behaviour is undetermined.
- Note 2:** On port pin P0.25 (when configured as general purpose input pin), leakage current increases when the input voltage is $V_i \geq V_{dd\ I/O} + 0.5\text{ v}$. Care must be taken to limit the current to less than 4 mA by using a series limiting resistor.