ERRATA SHEET

Date: **2010 February 9**
Document Release: **Version 1.4**
Device Affected: **LPC2460**

This errata sheet describes both the known functional problems and any deviations from the electrical specifications known at the release date of this document.

Each deviation is assigned a number and its history is tracked in a table at the end of the document.

NXP
Semiconductors

founded by Philips

Document revision history

Rev	Date	Description
1.4	20100209	Added date code info for IRC.2
1.3	20100122	Added Vbat.2
1.2	20090814	Added IRC.2
1.1	20090511	Added Rev D
1.0	20080812	First version

Identification

The typical LPC2460 devices have the following top-side marking:

LPC2460xxx

xxxxxxx

xxYYWW R[x]

The last/second to last letter in the third line (field ‘R’) will identify the device revision. This Errata Sheet covers the following revisions of the LPC2460:

Revision Identifier (R)	Comment
‘B’	Initial device revision
‘C’	Second device revision
‘D’	Third device revision

Field ‘YY’ states the year the device was manufactured. Field ‘WW’ states the week the device was manufactured during that year.

Errata Overview - Functional Problems

Functional Problem	Short Description	Device Revision the problem occurs in
Core.1	Incorrect update of the Abort Link register in Thumb state	'B', 'C', 'D'
CAN.1	Data overrun condition can lock the CAN controller	'B'
Vbat.1	Increased power consumption on Vbat when Vbat is powered before the 3.3 V supply used by rest of device	'B'
Vbat.2	The Vbat pin cannot be left floating	'B'

Errata Overview - AC/DC Deviations

AC/DC Deviation	Short Description	Device Revision the deviation occurs in
IRC.1	Accuracy of the Internal RC oscillator (IRC) frequency may be outside of the 4 MHz +/- 1 % specification only at extreme temperatures.	'C'
IRC.2	Accuracy of the internal RC oscillator (IRC) frequency for devices only with date codes 0949 and before are outside of spec between −20 °C and −40 °C	'D'

Errata Notes

Notes	Short Description	Device Revision the note applies to
Note 1	When the input voltage is Vi ≥ Vdd I/O + 0.5 v on each of the following port pins P0.23, P0.24. P0.25, P0.26, P1.30, P1.31, P0.12, and P0.13 (configured as general purpose input pin (s)), current must be limited to less than 4 mA by using a series limiting resistor.	'B', 'C', 'D'

Functional Problems of LPC2460

Core.1 **Incorrect update of the Abort Link register in Thumb state**

Introduction: If the processor is in Thumb state and executing the code sequence STR, STMIA or PUSH followed by a PC relative load, and the STR, STMIA or PUSH is aborted, the PC is saved to the abort link register.

Problem: In this situation the PC is saved to the abort link register in word resolution, instead of half-word resolution.

Conditions:

The processor must be in Thumb state, and the following sequence must occur:

<any instruction>

<STR, STMIA, PUSH> <---- data abort on this instruction

LDR rn, [pc,#offset]

In this case the PC is saved to the link register R14_abt in only word resolution, not half-word resolution. The effect is that the link register holds an address that could be #2 less than it should be, so any abort handler could return to one instruction earlier than intended.

Work around: In a system that does not use Thumb state, there will be no problem.

In a system that uses Thumb state but does not use data aborts, or does not try to use data aborts in a recoverable manner, there will be no problem.

Otherwise the workaround is to ensure that a STR, STMIA or PUSH cannot precede a PC-relative load. One method for this is to add a NOP before any PC-relative load instruction. However this is would have to be done manually.

CAN.1: **Data Overrun condition can lock the CAN controller**

Introduction: Each CAN controller provides a double Receive Buffer (RBX) per CAN channel to store incoming messages until they are processed by the CPU. Software task should read and save received data as soon as a message reception is signaled.

In cases, where both receive buffers are filled and the contents are not read before the third message comes in, a CAN Data Overrun situation is signaled. This condition is signaled via the Status register and the Data Overrun Interrupt (if enabled).

Problem: In a Data Overrun condition, the CAN controller is locked from further message reception.

Workaround: 1. Recovering from this situation is only possible with a soft reset to the CAN controller.

2. If software cannot read all messages in time before a third message comes in, it is recommend to change the acceptance filtering by adding further acceptance filter group(s) for messages, which are normally rejected. With this approach, the third incoming message is accepted and the Data Overrun condition is avoided. These additional messages are received with the corresponding group index number can be easily identified and rejected by software.

Vbat.1: **Increased power consumption on Vbat when Vbat is powered before the 3.3 V supply used by rest of the device.**

Introduction: The device has a Vbat pin which provides power only to the RTC and Battery RAM. Vbat can be connected to a battery or the same 3.3 V supply used by rest of the device (VDD(3V3) pin, VDD(DCDC)(3V3) pin).

Problem: If Vbat is powered before the 3.3 V supply, Vbat is unable to source the start-up current required for the Battery RAM. Therefore, power consumption on the Vbat pin will be high and will remain high until 3.3 V supply is powered up. Once 3.3 V supply is powered up, power consumption on the Vbat pin will reduce to normal and subsequent power cycle on the 3.3 V supply will not cause an increased power consumption on the Vbat pin.

Workaround: Provide 3.3 V supply used by rest of the device first and then provide Vbat voltage.

Vbat.2: The Vbat pin cannot be left floating

Introduction: The device has a Vbat pin which provides power only to the Real Time Clock (RTC) and Battery RAM. Vbat can be connected to a battery or the same supply used by rest of the device (VDD(3V3) pin, VDD(DCDC)(3V3) pin). The input voltage range on the Vbat pin is 2.0 V minimum to 3.6 V maximum for temperature -40 C to 85 C. Normally, if the RTC and the Battery RAM are not used, the Vbat pin can be left floating.

Problem: If the Vbat pin is left floating, the internal reset signal within the RTC domain may get corrupted and as a result, prevents the device from starting-up.

Workaround: The Vbat should be connected to a battery or the same supply used by rest of the device (VDD(3V3) pin, VDD(DCDC)(3V3) pin).

AC/DC Deviations

IRC.1 **Accuracy of the Internal RC oscillator (IRC) frequency may be outside of the 4 MHz +/- 1 % specification only at extreme temperatures.**

Introduction: The device has a 4 MHz internal RC oscillator (IRC) which can be optionally used as the clock source for the Watch Dog Timer (WDT), and/or as the clock that drives the PLL and subsequently the CPU. The IRC frequency spec is 4 MHz +/- 1 % accuracy over the entire voltage and temperature range. During In-System Programming (ISP), the auto-baud routine is expecting the IRC frequency to be 4 MHz +/- 1 % and is used to synchronize with the host via serial port 0.

Problem: On the LPC2460 Rev C device only, the accuracy of internal RC oscillator (IRC) frequency meets 4 MHz +/- 1 % specification only at room temperature however, at extreme temperatures, the accuracy of internal RC oscillator (IRC) frequency may be 4 MHz +/- 10 %. As a result, at extreme temperatures, this may affect the auto-baud routine's ability to synchronize with the host via serial port 0 during In-System Programming (ISP) at higher baud rates.

Work around: None

IRC.2 **Accuracy of the Internal RC Oscillator (IRC) frequency for devices only with date codes 0949 and before are outside of the 4 MHz +/− 1 % specification only at temperatures between −20 °C and −40 °C.**

Introduction: The device has a 4 MHz internal RC oscillator (IRC) which can be optionally used as the clock source for the Watch Dog Timer (WDT), and/or as the clock that drives the PLL and subsequently the CPU. The IRC frequency spec is 4 MHz +/− 1 % accuracy over the entire voltage and temperature range. During In-System Programming (ISP), the auto-baud routine is expecting the IRC frequency to be 4 MHz +/− 1 % and is used to synchronize with the host via serial port 0.

Problem: On the LPC2460 Rev D device (only with date codes 0949 and before), the accuracy of internal RC oscillator (IRC) frequency does not meet the 4 MHz +/− 1 % specification for temperatures between −20 °C and −40 °C and the accuracy of internal RC oscillator (IRC) frequency is 4 MHz +/− 5 % instead. As a result, only at these temperatures, this may affect the auto-baud routine's ability to synchronize with the host via serial port 0 during In-System Programming (ISP) at higher baud rates. For temperatures above −20 °C, the accuracy of internal RC oscillator (IRC) frequency meets the 4 MHz +/− 1 % specification.

Work around: None

Errata Notes

Note 1: On each of the following port pins P0.23, P0.24. P0.25, P0.26, P1.30, P1.31, P0.12, and P0.13 (when configured as general purpose input pin (s)), leakage current increases when the input voltage is Vi ≥ Vdd I/O + 0.5 v. Care must be taken to limit the current to less than 4 mA by using a series limiting resistor.