

# ERRATA SHEET

**Date:** 2007 Jul 18  
**Document Release:** Version 1.2  
**Device Affected:** P89LPC924

This errata sheet describes both the functional deviations and any deviations from the electrical specifications known at the release date of this document.

Each deviation is assigned a number and its history is tracked in a table at the end of the document.

2007 Jul 18

**Identification:**

The typical P89LPC924 devices have the following top-side marking:

P89LPC924x x  
xxxxxxx xx  
xxYYWW R

The last letter in the third line (field 'R') will identify the device revision. This Errata Sheet covers the following revisions of the P89LPC924:

Revision Identifier (R)	Comment
'A'	Initial device revision
'B'	Updated device revision

Field 'YY' states the year the device was manufactured. Field 'WW' states the week the device was manufactured during that year.

**Errata Overview - Functional Problems**

Functional Problem	Short Description	fixed in revision	added
ADC.1	Single Step mode multi channel boundary interrupt	none	v1.0
ADC.2	Timer/Edge with Scan Mode Counter Reset	B	v1.0
DIVM.1	Using DIVM in power-down mode	none	v1.2
I/O.1	Port 3.0 can be an output during a power-up cycle	none	v1.2
RESET.1	External reset does not function correctly when using DIVM	none	v1.2
UART.1	Breakdetect trips after 10 zero bits	none	v1.2

**Errata Overview - AC/DC Deviations**

AC/DC Deviation	Short Description	fixed in revision	added
-	-	-	-

**Errata Notes**

Note	Short Description	added
V <sub>DD</sub> .1	V <sub>DD</sub> Power cycling.	v1.0
IRC.1	Internal RC oscillator accuracy	v1.1

## Functional Deviations of P89LPC924

### ADC.1: Single Step mode multi channel boundary interrupt

**Introduction:** The ADC on the LPC924 is an Analog to Digital converter with 8 bits of resolution. The ADC has features such as a Single Step mode where the ADC will step through the selected channels on each ADC start condition.

**Problem:** When the ADC is in Single Step mode with more than 1 channel selected, and a boundary interrupt occurs to any of the lower selected channel-bits, a write to the ADMODA register to clear the BNDI bit before all the selected channels are converted will reset the channel selection counter and the ADC will go back and wait at the lowest selected channel for the next conversion. .

**Workarounds:**

- 1) Clear the lower channel bits including the boundary interrupted channel in ADCINS register before the next start request.
- 2) Use the default boundary channel, not clear BNDI bit until all channels are converted.

### ADC.2: Timer/Edge trigger with scan mode

**Introduction:** The ADC on the LPC924 is an Analog to Digital converter with 8 bits of resolution. The ADC has features such as a Timer / Edge trigger mode where the ADC will generate an ADC start condition on the timer or edge on a pin. Scan mode is an ADC feature where the ADC will scan through all selected channels on an ADC start condition.

**Problem:** When the ADC is in Timer or Edge mode, with scan mode, and more than 1 channel is selected, and the repeat conversion on timer or edge is selected, the channel counter increments to last selected channel on first conversion, but on all subsequent conversion triggers the counter is not reset, so only the last channel is converted over and over again.

**Workarounds:**

- 1) To reset the counter that sticks on the last channel the ADC can be disabled and enabled again.
- 2) Switch from ADC mode to DAC mode and back.

### DIVM.1: Using DIVM in power-down mode

**Introduction:** The LPC924 has a DIVM register that can be used to divide the cclk down. Using DIVM can greatly reduce power when in active mode.

**Problem:** When DIVM is used in active mode and power-down mode is then entered the LPC924 can not be waken up from power down mode.

**Workaround:** Before entering powerdown mode set DIVM back to 0x00. This way the LPC924 will be operating full speed for one instruction before entering power-down mode. After the LPC924 has been waken up DIVM can be set back to its original value.

**I/O.1: Port 3.0 can be an output during a power-up cycle**

**Introduction:** The LPC924 can be selected to be clocked by an internal RC oscillator. When the internal RC oscillator is selected, P3.0 and P3.1 (which would be used for the crystal oscillator circuit) pins can now be used as general purpose IO pins.

**Problem:** When the LPC924 is powered up the configuration of the UCFG1 is read out and the LPC924 configured accordingly. The UCFG1 gets read out on the low brownout level of the LPC924 (typically around 2.3V). Before the UCFG1 is read out the crystal oscillator circuit might be enabled. When the crystal circuit is enabled P3.0 is driven to the inverse state of P3.1.

**Workaround:** Please make sure your external circuitry connected to P3.0 is not affected by this behaviour. Otherwise it is recommended to switch to a different port pin.

**RESET.1: External reset does not function correctly when using DIVM**

**Introduction:** The LPC924 can be set up to use either an internal reset or an external reset pin on P1.5. The DIVM register can be used to divide down the internal CCLK down.

**Problem:** When the LPC924 is configured to have an external reset pin on P1.5 and in the program the DIVM register is programmed to a value different from 0x00 to slow down CCLK, then the next reset pulse will not generate a proper reset for the LPC924. A power cycle has to be applied for the LPC924 to start up again properly.

**Workaround:** Use the internal reset function.

**UART.1: Breakdetect trips after 10 zero bits**

**Introduction:** The UART on the LPC924 has the ability to detect a breakdetect signal, a break signal is a 11 bit long low signal on the RxD input of the UART.

**Problem:** The breakdetect flag will be set after 10 low bits on the RxD input of the UART. When 9 bit mode is used and all 9 data bits are 0 and the start bit is zero this will be detected as a breakdetect.

**Workaround:** No known workaround.

## **Electrical and Timing Specification Deviations of P89LPC924**

**No known errata**

## Errata Notes

### **V<sub>DD</sub>.1: V<sub>DD</sub> Power cycling**

To generate a proper Power-On-Reset (POR), V<sub>DD</sub> must have dropped below 0.2V before being powered back up. Power-cycling without V<sub>DD</sub> having dropped below 0.2V may result in incorrect Program Counter values.

Please also see the V<sub>POR</sub> specification in LPC924 Datasheet, DC electrical characteristics. Section 8.15 (Reset) states that during a power cycle, V<sub>DD</sub> must fall below V<sub>POR</sub>.

### **IRC.1: Internal RC oscillator accuracy**

To be able to guarantee the Internal RC oscillator accuracy over the full operating range the V<sub>DD</sub> supply has to be decoupled sufficiently. Sufficient decoupling is dependant on the noise level in the application, typically a 0.1uF should be sufficient for most applications.

Noise on the V<sub>DD</sub> supply pins can cause the Internal RC oscillator to go slightly outside of the specified range.