

TN09001

Differentiated features of the LPC1700 series of Cortex-M3 microcontrollers

Rev. 02 — 9 April 2009

Technical note

Document information

Info	Content
Keywords	LPC1700 Cortex-M3

Revision history

Rev	Date	Description
02	20090409	Removed reference to Deep power-down mode.
01	20090327	Initial version.

Contact information

For additional information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

1. Introduction

The NXP LPC1700 series of ARM Cortex-M3 microcontrollers has several new features that differ from the popular LPC2000 ARM7 MCUs and some of which are unique to NXP's implementation of the M3 core. This document will detail those unique features to help the user identify opportunities to utilize the tremendous performance of the LPC1700 family.

These features include:

- Flash Accelerator, which allows for execution of code with zero wait states at up to the maximum clock speed of 100 MHz
- General Purpose DMA for transfers between memories and supported peripherals
- Nested Vectored Interrupt Controller for interrupt handling
- Memory Protection Unit for critical code protection from accidental over-writes
- Wake-up Interrupt Controller for waking the CPU from deep sleep modes only on selected priority interrupts

1.1 Flash Accelerator

The LPC1700 series runs up to 100 MHz, making it the fastest Cortex-M3 microcontroller available. The flash accelerator block in the LPC1700 is an enhancement of the LPC2000 Memory Accelerator Module, which maximizes the performance and reduces power consumption of the Cortex-M3 processor running code from flash memory. The flash accelerator also provides speed and power improvements for data accesses to the flash memory.

The Cortex-M3 provides a separate bus for instruction access (Icode) and data access (Dcode) in the memory space. The flash accelerator includes an array of eight 128-bit buffers to store both instructions and data. During linear code execution, the next four 32-bit instructions are stored in the code instructions buffer. Other buffers are used for storing instructions and data at code branches. The replacement strategy of the flash accelerator attempts to maximize the chances that potentially reusable information is retained until it is needed again.

1.2 DMA

In addition to the Flash Accelerator, the General Purpose Direct Memory Access (GP DMA) is perhaps the most unique and differentiated feature on the LPC1700 series. The GP DMA has been designed to give the User the most flexibility and performance to avoid the bottlenecks apparent on competitive M3 DMAs. The NXP 8-channel DMA enables peripheral-to-memory, memory-to-peripheral, peripheral-to-peripheral, and memory-to-memory transactions with 16 DMA request lines. The source and destination areas can each be either a memory region or a peripheral. The DMA controller also allows data transfers between the USB and Ethernet controllers and the three separate on-chip SRAM areas. The DMA supports SSP0/1, all UARTs, the I2S-bus interface, the ADC, the DAC, General Purpose I/O and two match signals for each timer, which can be used to trigger DMA transfers

Other DMA features include scatter or gather so the source and destination areas do not have to occupy contiguous areas of memory, hardware channel priority, programmable burst size internal four-word FIFO per channel.

1.3 Nested Vectored Interrupt Controller (NVIC)

The ARM7TDMI does not have an interrupt controller as part of the core. To handle interrupts, ARM7TDMI microcontrollers, including the LPC2000 from NXP, add a Vectored Interrupt Controller (VIC) on the AHB bus. This results in an interrupt latency of 24-42 cycles and 16 cycles to return from servicing. The Cortex-M3 has an integrated interrupt controller called the Nested Vectored Interrupt Control (NVIC). The NVIC provides for faster, more deterministic interrupt latencies. Interrupts always take just 12 cycles and then 12 cycles to return from servicing.

In the LPC1700, the NVIC supports 33 vectored interrupts, with 32 programmable interrupt priority levels and hardware priority level masking. The NVIC also has a relocatable vector table, a non-Maskable Interrupt and software interrupt generation.

The ARM7 processor used the banked shadow register exception model, while the Cortex-M3 has a stack based exception model. To make application development easier, the LPC1700 handles the stack operations in hardware. This eliminates the need to write assembler wrappers to perform stack manipulation.

The NVIC also supports tail-chaining, which handles back-to-back interrupts, without repeating the complete state save and restore cycle. Tailchaining achieves much lower latency with a simple 6 cycle instruction fetch instead of the serial stack pop and push actions that normally take over 30 clock cycles. The processor state is automatically saved on interrupt entry, and restored on interrupt exit.

The NVIC is also involved in the power-management of the integrated sleep modes, such as the Sleep On Exit mode, in which the microcontroller moves into low-power mode as soon as it exits the lowest priority interrupt-service routine and stays in sleep state until another exception is encountered.

The NVIC also integrates a System Tick (SysTick) timer, a 24-bit down timer that is ideal for a Real Time Operating System or other scheduled tasks because it can generate interrupts at regular time intervals.

1.4 Memory Protection Unit (MPU)

The MPU is an optional component of the Cortex-M3 processor but is included on all LPC1700 microcontrollers and is currently not included in competitive M3 microcontrollers. The MPU is used to protect critical data from being overwritten by user applications. Applications can be broken into separate processing tasks with its own memory (code, data, stack, and heap) which prevents access to each other's data, disables access to memory regions, allows memory regions to be defined as read-only and detects unexpected memory accesses, all of which improves the reliability of the system. The MPU supports up to 8 regions each of which can be divided into 8 sub-regions.

1.5 Wake Up Interrupt Controller (WIC)

The Wakeup Interrupt Controller (WIC) is a new feature that has been added to the Cortex-M3 Release 2 and is not available on Release 1 versions. All NXP M3 MCUs use Cortex-M3 Release 2 and include the WIC, which allows the CPU to automatically wake up from any enabled priority interrupt while the clocks are stopped in Deep sleep and Power-down modes. The Nested Vectored Interrupt Controller (NVIC) sends a mask to the WIC of all of the interrupts that are both enabled and have been given priority by the User for immediate servicing. With this mask, the WIC only wakes up the CPU when one

of the interrupts has occurred. This saves power by eliminating the need to periodically wake up the CPU to poll the interrupts.

For ultra-low power applications, it is desirable to be able to significantly reduce the dynamic and static power of the processor while in very-deep-sleep modes. Stopping clocks and/or removing power from the processor can achieve this. The NVIC is unable to prioritize or detect interrupts while powered off, so knowing when to come out of very-deep-sleep is impossible without enabling the CPU and wasting power. The WIC can emulate the full NVIC behavior on entry to very-deep-sleep and uses minimal power, enabling it to always remain powered in very-deep-sleep mode.

1.6 Trace and Debug Features

The NXP LPC1700 has an extensive set of debug features. The Cortex-M3 processor has integrated two types of debugging modes: standard JTAG and ARM Serial Wire Debug (SWD). The SWD is a two-pin debugging mode that uses only a clock and data interface. The LPC1700 supports both debugging mode types, unlike some competitive M3 MCU offerings. The LPC1700 debugging features include direct debug access to all memories, registers, and peripherals, in which no target resources are required for the debugging session. Also, a trace port is included that provides CPU instruction trace capability, with output through a 4-bit trace data port or the SWD. The LPC1700 includes eight Hardware Breakpoints with six instruction breakpoints that can also be used to remap instruction addresses for code patches. There are also four data Watchpoints that can also be used as trace triggers. Finally, there is an included Instrumentation Trace Macrocell that allows additional software controlled trace to simplify debugging of application code. The Instrumentation Trace Macrocell is an optional component of the Cortex-M3 and is uniquely included by NXP on the LPC1700 series.

Trace can be done using either a 4-bit parallel interface or the Serial Wire Output. When the Serial Wire Output is used, less data can be traced, but only two pins are used, while parallel trace has a greater bandwidth, but uses 5 functional pins that may be needed in the application. Note that the trace function available for the Cortex-M3 is functionally very different than the trace that was available for previous ARM7 based devices, using only 5 pins instead of 10.

2. Legal information

2.1 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

2.2 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of a NXP Semiconductors product can reasonably be expected

to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is for the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

2.3 Trademarks

Notice: All referenced brands, product names, service names and trademarks are property of their respective owners.

3. Contents

- 1. Introduction3**
- 1.1 Flash Accelerator3
- 1.2 DMA3
- 1.3 Nested Vectored Interrupt Controller (NVIC).....4
- 1.4 Memory Protection Unit (MPU).....4
- 1.5 Wake Up Interrupt Controller (WIC)4
- 1.6 Trace and Debug Features.....5
- 2. Legal information6**
- 2.1 Definitions.....6
- 2.2 Disclaimers.....6
- 2.3 Trademarks6
- 3. Contents.....7**

Please be aware that important notices concerning this document and the product(s) described herein, have been included in the section 'Legal information'.

© NXP B.V. 2009. All rights reserved.

For more information, please visit: <http://www.nxp.com>
 For sales office addresses, email to: salesaddresses@nxp.com

