



LPC2400 & LPC2300 Series Ethernet, USB, CAN & LCD

Business Line Standard IC's
Product Line Microcontrollers



The ARM7TDMI-S core

ARM7TDMI-S

- ▶ T - Thumb architecture extension
- ▶ D - Debug extensions
- ▶ M - Enhanced multiplier (32x8) with 64-bit result option
- ▶ I - EmbeddedICE Macrocell™
- ▶ S - Fully synthesizable (soft IP)

The ARM7 Core

- ▶ Reduced Instruction Set Computer (RISC)
 - Simple instruction set and decode compared to CISC processors
 - Allows for high instruction throughput and real-time interrupt response
- ▶ 3-stage pipeline
 - Fetch, Decode and Execute
 - All parts of the processing and memory systems can operate continuously
- ▶ Von Neumann architecture
 - Single path for Instructions and Data
 - Data Bypass buffer of MAM reduces bottlenecks

ARM state and Thumb state

- ▶ ARM uses a 32-bit architecture with a subset of 16-bit instructions, still using 32-bit data and registers.
- ▶ Set of instructions re-coded into 16 bits
 - Improved code density by ~ 30%
 - saving program memory space
- ▶ In Thumb state only the program code is 16-bit wide
 - after fetching the 16-bit instructions from memory, they are decompressed to 32 bit instructions before they are decoded and executed
 - all operations are still 32-bit operations

8-bit & 16-bit code size vs Thumb

NXP LPC2000 (Thumb Mode)	26796 bytes
Renesas H8	37921 bytes
Renesas M16C	26743 bytes
TI MSP430	26424 bytes
Atmel AVR	26055 bytes
Freescale HCS12	23916 bytes

1. Test code was a well known communications protocol stack that was written to run on any target platform from desktops to embedded systems. Code is entirely ANSI C.
2. Code used "as is." No effort was made to optimize the code for any particular target or intrinsic data size.
3. All results obtained using IAR cross compilers for respective targets
4. IAR implies no endorsement of any particular device by these results
5. All results achieved using latest version of IAR compilers as of June '05
6. All results achieved using maximum optimization for code size
7. Results are for code size only, no constant data

Source: IAR June 2005

System Control

Vectored Interrupt Controller (VIC)

- ▶ ARM core has only 2 interrupt inputs
 - Fast Interrupt Request (FIQ) are the highest priority
 - Interrupt Request (IRQ) have programmable priority
- ▶ VIC assigns up to **32 interrupts** as FIQ or vectored IRQ types
 - Allows interrupts to be prioritized dynamically with **16 levels**
- ▶ Each peripheral device has one interrupt line connected to the VIC
 - Each peripheral may have several interrupt flags
 - Individual interrupt flags may also represent more than one source
- ▶ Any pin on PORT0 and PORT2 can generate interrupt
 - Interrupts on rising edge, falling edge or both

Phase Locked Loop (PLL)

- ▶ 32 KHz to 50 MHz input clock frequency
- ▶ Output frequency from 10 MHz up to the maximum CPU rate
- ▶ Programmable frequency multiplication (x1, x2, x3, x4,, x31, x32)
- ▶ PLL is turned off and bypassed following a chip Reset and when by entering power down mode
- ▶ PLL must be enabled by software
- ▶ PLL lock indicator can be used as an interrupt to connect the PLL once it is locked
- ▶ PLL programming requires a special feed sequence (similar to the watchdog) for safety

Reset and Brown Out Detect

- ▶ Up to four Reset sources:
 - RESET pin which is a Schmitt trigger input pin
 - Watchdog (WDT) reset
 - Power-On (POR) reset
 - Brown Out Detection (BOD) circuit
- ▶ Brown Out Detect: 2-stage monitoring.
 - If 3.3V pin falls below 2.95 V, the BOD asserts interrupt or flag.
 - If 3.3V pin falls below 2.65 V, BOD stops Flash from being written
 - Both thresholds include some hysteresis.

Power Modes

▶ Power options:

- On-chip DC-DC converter supplies 1.8V power to all internal logic, except in the RTC power domain.
- Power can be adjusted by changing clock sources, reconfiguring PLL values, and/or altering the CPU clock divider value
- Ability to divide down or shut off clocks to individual on-chip peripherals

▶ Power reduction modes:

- **Idle:** CPU stopped; Peripherals running
- **Sleep:** MCU receives no internal clocks. The processor state and registers, peripheral registers, and internal SRAM values are preserved and logic levels remain static. PLL is disconnected. Flash and RTC remains on (unless User disabled). With IRC, code executes in 4 clock cycles!
- **Power Down:** Same as Sleep mode except Flash and RTC are off. With IRC, code executes from SRAM in 60 us + 4 clock cycles

Emulation and Debugging

- ▶ **EmbeddedICE** provides on-chip debug support.
 - Allows the software debugger to examine or insert instructions via JTAG port directly to the core.
 - Allows instructions to execute at a slow debug speed or at a fast system speed
 - The ARM core allows communication with the host without affecting the normal program flow or even entering the debug state
- ▶ **Embedded Trace Module (ETM)** provides real-time trace capability, outputting information about processor execution to a trace port
 - A software debugger allows configuration of the ETM using a JTAG interface and displays the trace information that has been captured
 - Instruction trace is significantly compressed by only broadcasting branch addresses as well as a set of status signals that indicate the pipeline status on a cycle by cycle basis
- ▶ **RealMonitor** is a debug monitor that runs in the background while users debug their foreground application, enabling real-time debug

Flash and SRAM

Best Flash in the Market

“In all seven benchmark tests, the NXP LPC2129 showed a consistent performance edge of 37 percent to 51 percent compared with the other ARM7-based devices, demonstrating the impact of the LPC2129’s optimized flash interface.”

-November 8, 2006: EEMBC® Scores for NXP’s ARM7-Based LPC2129 Show Dramatic Effect of Memory Subsystem on Microcontroller Performance

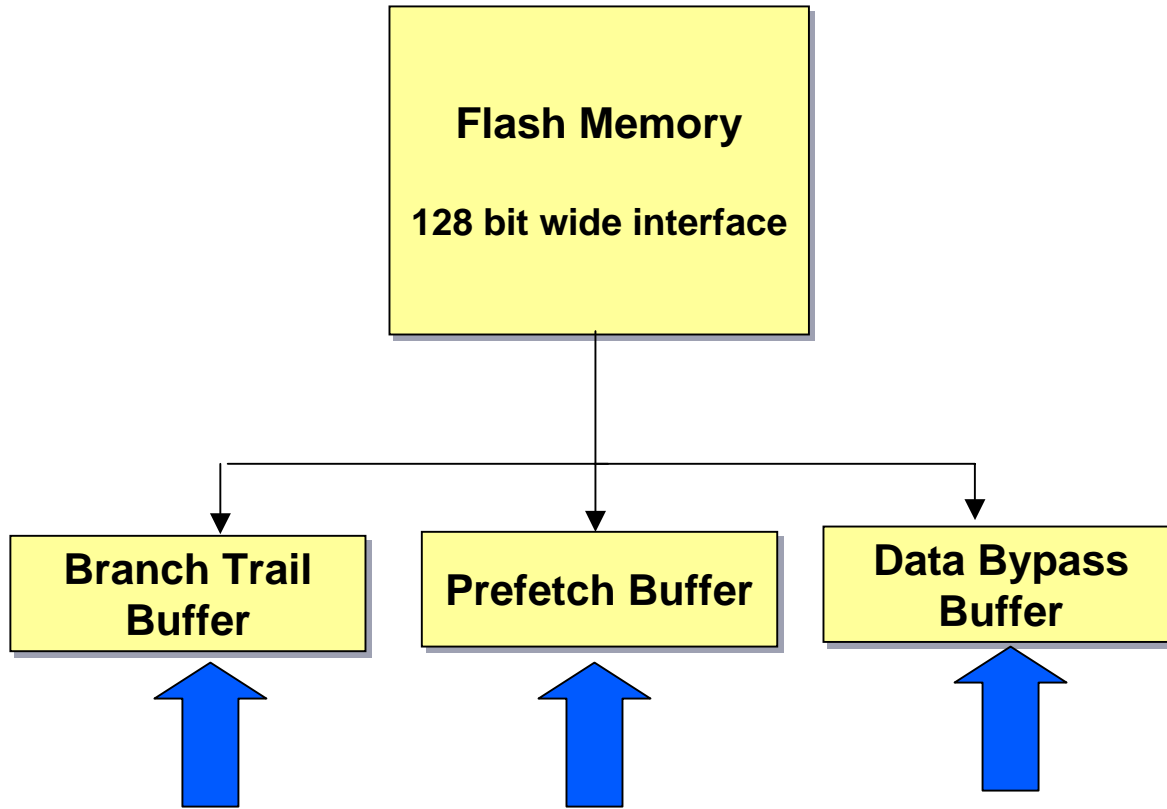
<http://www.eembc.org/>



Memory Accelerator Module (MAM)

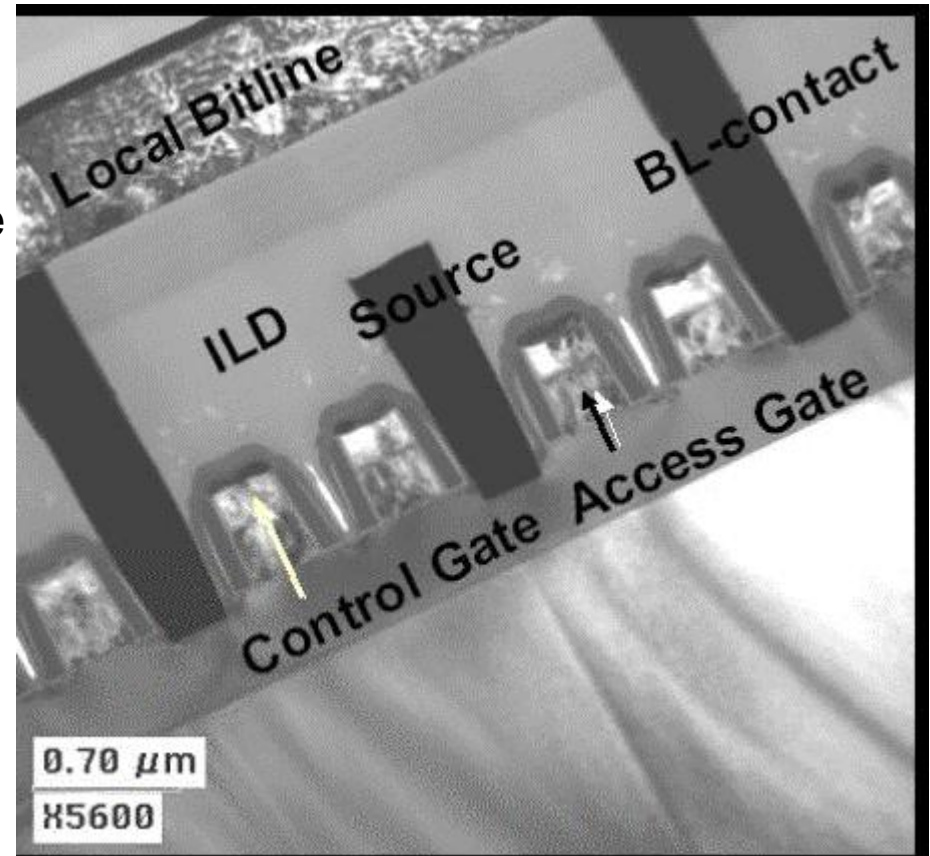
- ▶ Why is a MAM needed?
 - Normal Flash access time is approximately 50ns
 - Without MAM, execution out of Flash with zero wait states is 20 MHz max
 - Users want direct execution out of Flash up to 72 MHz
- ▶ Why not a cache?
 - Cache is difficult to implement
 - Performance of Cache is difficult to predict
 - In many applications predictability, determinism and repeatability are important features
- ▶ MAM Features
 - Retains Determinism
 - MAM allows clock cycles to be pre-determinable before Run-Time & countable by Tool chain utility
 - Allows Operation at up to 72 MHz with a 20 MHz Flash Array, can be enabled or disabled and has different programmable modes

Memory Accelerator Module (MAM)



NXP Innovation in Embedded Flash

- **Best-in-class** 0.14mm 6 Metal eFlash Technology in Nijmegen, The Netherlands & SSMC in Singapore
- 2T NOR cell for robustness, Automotive qualified Flash
- **Very low power**; Read operation down to 1.2V
- 128-bit wide word with 8-bit ECC for single-bit error correction
- Very **high bandwidth** with Memory Accelerator architecture
- On-chip Flash is secure



Zero wait-state operation from Flash up to 72 MHz

Code Read Protection (CRP)

- ▶ User can enable different levels of security so that access to the on-chip Flash and use of the JTAG and ISP can be restricted. There are three levels of the Code Read Protection:
- ▶ **CRP1** disables access to chip via the JTAG and allows partial Flash update using a limited set of the ISP commands
 - This mode is useful when CRP is required and Flash field updates are needed but all sectors cannot be erased
- ▶ **CRP2** disables access to chip via the JTAG and only allows full Flash erase and update using a reduced set of the ISP commands
- ▶ **CRP3** fully disables any access to chip via the JTAG pins and the ISP

SRAM

- ▶ RAM may be used for code and/or data storage
- ▶ May be accessed as 8 bits, 16 bits, and 32 bits
- ▶ 16 KB SRAM buffer for the Ethernet and 16 KB SRAM for USB/LCD can also be used for data and/or code storage
- ▶ The 2 KB of RTC SRAM can only be used for data storage
- ▶ RTC SRAM is battery powered and retains the content in the absence of the main power supply

Peripherals

With a single bus, the CPU, Ethernet, USB and LCD all contend for bandwidth, causing a communications “traffic jam”



The solution is the NXP LPC2300/2400 series

Independent Buses

- ▶ With independent Local, AHB1 and AHB2 buses, concurrent operations become possible
- ▶ Local Bus connects CPU with zero wait-state Flash
 - CPU Instruction Fetch
- ▶ AHB1 bus support USB OTG/OHCI/Device and LCD
 - USB packet reception and transfer to SRAM
 - 4 KB FIFO Buffer for USB
 - LCD frame transfer from internal or external SRAM
 - 16 KB SRAM for USB or LCD buffering of heavy traffic
 - USB DMA and LCD DMA
- ▶ AHB2 Dedicated to Ethernet
 - Ethernet packet reception and transfer to SRAM
 - 16 KB SRAM for Ethernet buffering
 - Ethernet DMA

LPC2300/2400 Peripherals

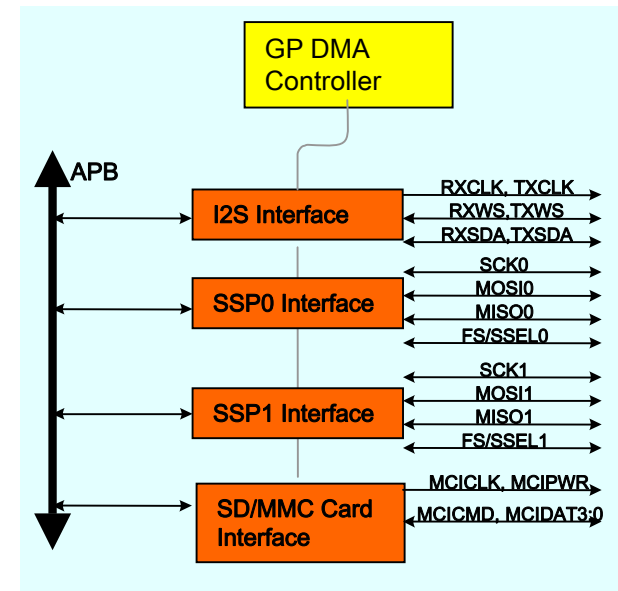
- ▶ 10/100 Ethernet
 - Built in MAC with MII and RMII interfaces to external PHY
 - 16 KB SRAM for heavy traffic buffering
 - Ethernet DMA
- ▶ USB 2.0 Full Speed On-The-Go/Open Host Control Interface/Device
 - Built in Device and OHCI PHY
 - USB DMA
 - 16 KB SRAM Buffer + 4 KB FIFO
 - Supports 32 endpoints and all transfer modes
- ▶ CAN 2.0B
 - Two channels
 - Built-in Hardware Acceptance Filters
- ▶ I²S interface
- ▶ Three I²C interfaces, SSP, SSP/SPI interfaces
- ▶ Four 16C550-type UARTs
 - Includes fractional baud rate generator, auto-baud & hardware flow control

LPC2300/2400 Peripherals (continued)

- ▶ SD/MMC memory card interface
- ▶ 6-channel, 10-bit A/D Converter,
- ▶ 10-bit D/A Converter
- ▶ 4 MHz on-chip RC-oscillator trimmed to 1% accuracy
 - Can be used as Main Clock via PLL
- ▶ Four 32-bit general purpose timers
 - Each with 4 Capture, 4 Compare and 4 external outputs
- ▶ Watchdog timer from multiple clock source options
- ▶ PWM block supporting 3 Phase Motor Control with “dead time” generation
- ▶ Low-power Real Time Clock with 2 KB SRAM and battery back-up
- ▶ 160 Fast general purpose I/O lines
 - All pins on Port 0 and Port 2 can be used as external interrupts (rising, falling or both)
- ▶ Single 3.3V power supply (3.0 to 3.6V)

General Purpose DMA

- ▶ General Purpose two-channel DMA supports high-speed peripherals as well as memory-to-memory transfers
 - 32-bit AHB master bus width (support 8-, 16-, or 32-bit transfers)
 - Internal four-word FIFO per channel
- ▶ Can be used with SD/MMC, two SSP and the I²S interface
 - Connect peripherals to each other or to memory
- ▶ Flexible, customizable DMA performance
 - Big-endian and little-endian support
 - Programmable DMA burst size
 - Hardware DMA channel priority
 - Can generate interrupts



LPC2400 External Memory Interface

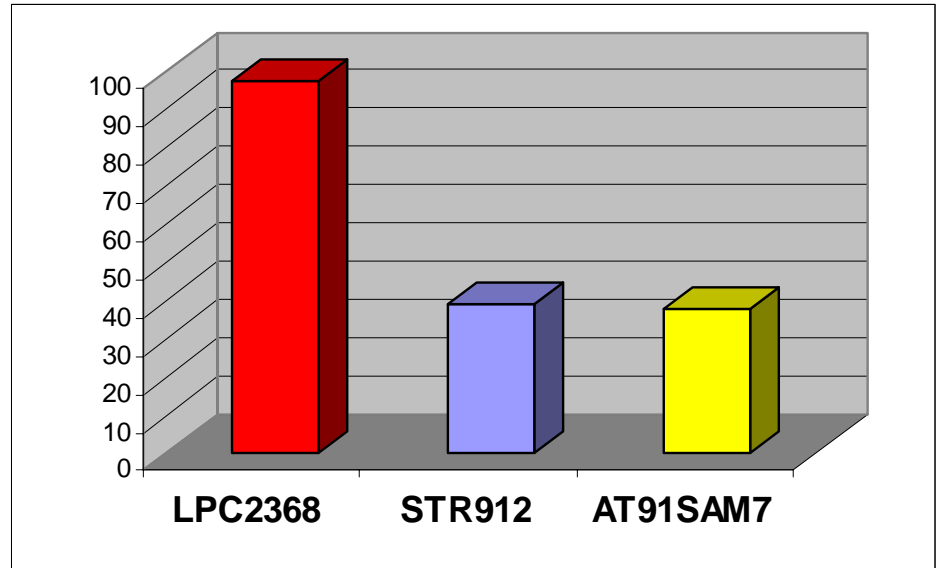
- ▶ MultiPort Memory Controller peripheral that offers support for SRAM, ROM, Flash, and memory-mapped peripherals
 - Four chip selects each for synchronous and static memory devices
 - Supports 2K, 4K, and 8K row address synchronous memory parts
 - Asynchronous page mode read
 - Programmable Wait States
 - Bus turnaround delay
 - Output enable and write enable delays
 - Extended Wait
- ▶ Also supports SDRAM with 16-bit and 32-bit wide chip select
 - Power saving modes control CKE and CLKOUT
 - Self-refresh mode controlled by software
- ▶ Read and Write buffers improve performance and reduce latency
- ▶ 8/16/32 data lines and 24 address lines

10/100 Ethernet MAC

- ▶ Independent (but not isolated), second AHB bus
- ▶ Supports 10/100 Ethernet PHY devices, including:
 - 10 Base-T
 - 100 Base-TX (Level 5 Unshielded Twisted Pair cable)
 - 100 Base-FX (Fiber Optic cable)
 - 100 Base-T4 (Level 3 UTP cable)
- ▶ Reduced Media Independent Interface (RMII) bus
 - 2-bit Data RX/TX paths: 10 Pins
- ▶ Media Independent Interface (MII) bus
 - 4-bit Data RX/TX paths, Data Valid, Collision Detect, Transmit Clock, Transmit error: 18 Pins
- ▶ Fully Compliant with IEEE 802.3X PAUSE MAC Control protocol
 - Full Duplex Flow Control (prevents the loss of outgoing packets during transmission if the switch is sending packets faster than the attached device can receive and process them by sending pause-control frames when its port buffer becomes full)
 - Half Duplex Back Pressure (ensures retransmission of incoming packets if unable to receive incoming packets)

Benchmark results using CMX RTOS

- Test performed on existing Development Boards
- CMX-MicroNet v3.08b THUMB Mode
- Speed = MBits/sec = Ethernet throughput numbers are calculated by timing the transmission of 1000 UDP packets containing 1460 bytes of data



http://www.cmx.com/mnspec_arm7.htm

USB 2.0

- ▶ Since USB is a standard, doesn't that make all microcontrollers with USB the same?

NO!!

- ▶ Architectural choices and implementation details make a big difference in performance and ease of use
- ▶ **NXP has the only fully-compliant USB available for ARM7 Microcontrollers**
 - Supports 16 Bi-directional endpoints
 - Supports all Transfer Modes and Maximum Buffers
 - Only USB to meet full frame bandwidth per transfer

USB Host/ On-The Go

▶ USB Host

- Enables full- and low-speed data exchange with USB devices attached to the bus. It consists of register interface, serial interface engine and DMA controller
- OHCI compliant
- Two downstream ports
- Supports per-port power switching

▶ USB OTG

- Integrates the host controller, device controller, and a master-only I2C interface to implement OTG dual-role device functionality. The dedicated I2C interface controls an external OTG transceiver
- Fully compliant with On-The-Go supplement to the USB 2.0 Specification
- Hardware support for Host Negotiation Protocol (HNP).
- Includes programmable timer for HNP and Session Request Protocol (SRP)
- Supports any OTG transceiver compliant with the OTG Transceiver Specification

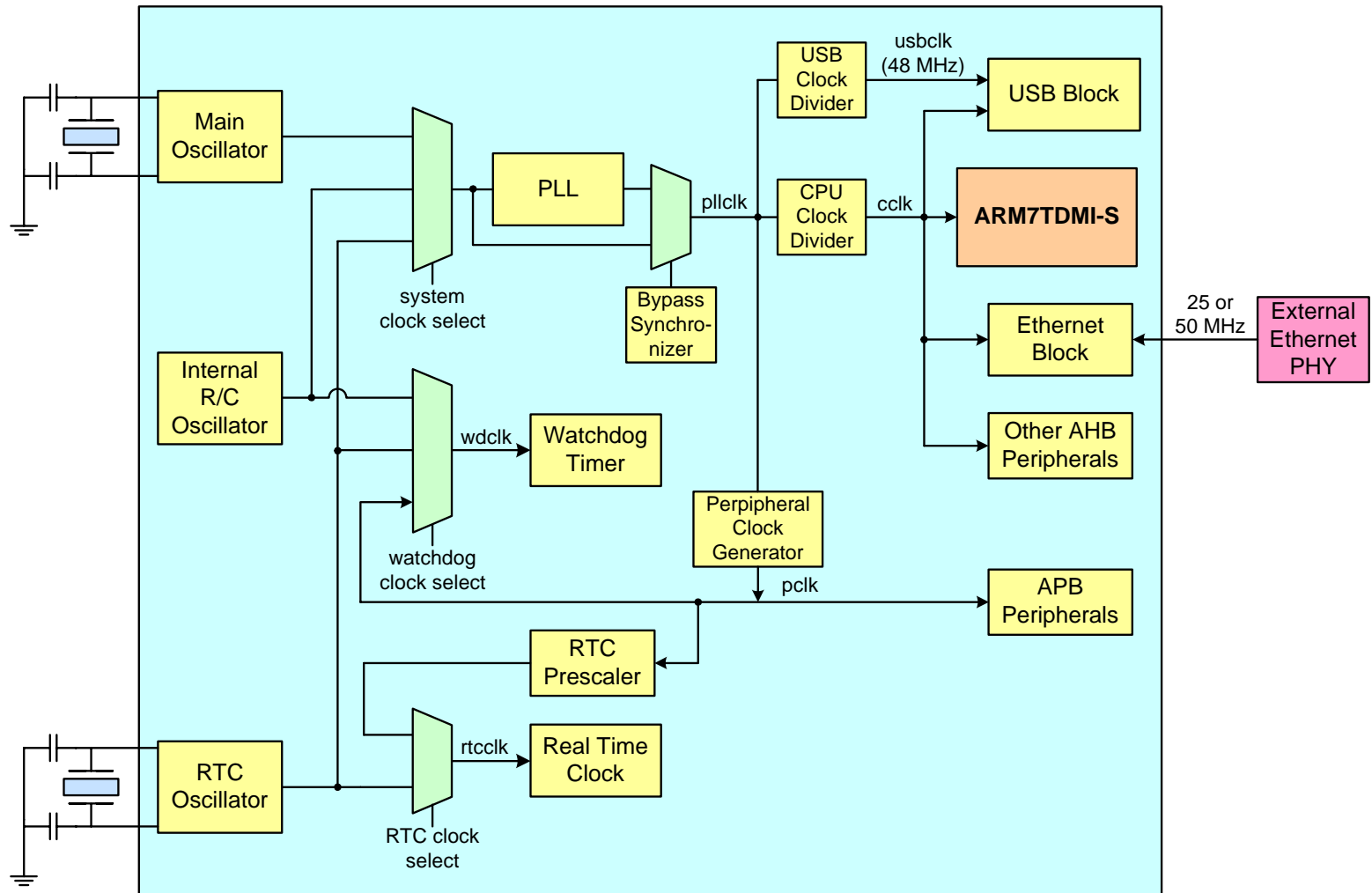
LPC247x Color LCD Controller

- ▶ Resolution up to 1024x768
- ▶ Single and dual panel Super Twisted Nematic (STN)
 - Monochrome displays with 4 or 8 bit interfaces
 - 1, 2 or 4 bits-per-pixel (bpp) monochrome palettes
 - Color displays with 1, 2, 4 or 8bpp color palettes
 - 15 level grey-scale, 3375 color display modes
 - 16 bpp direct true-color
- ▶ Thin Film Transistor (TFT) color displays
 - 32K color display modes
 - 1, 2, 4 or 8bpp color palettes
 - 16 bpp or 24 bpp direct true-color
- ▶ Hardware Cursor support for single panel displays.
- ▶ Resistive Touchscreen capability
- ▶ The LCD controller is connected to the AHB1 bus, so it processes Frame data independently of the Ethernet (AHB2 bus) and Flash (Local bus)

Clocks

- ▶ Main Oscillator
 - Operates with external crystal frequencies of 1MHz to 25 MHz
 - Can be used as main CPU clock with or without PLL
- ▶ Internal RC Oscillator (IRC)
 - Nominal 4 MHz, trimmed to 1% accuracy
 - May be used as main CPU clock with or without PLL
 - Used as main clock on power-up
- ▶ Real Time Clock (RTC)
 - Operates off of 32.768 KHz external crystal or from main oscillator
 - Can be used as clock source for RTC and/or Watch Dog Timer
 - May be used to clock CPU via the PLL
 - Powered by VBAT pin, connected to battery or 3.3V supply
 - 2 KB Battery RAM can be kept alive during deep power down
 - RTC alarm output can wake part from power down state
- ▶ Watch Dog Timer (WDT)
 - Programmable 32-bit timer with internal prescaler
 - Sourced from RTC clock, the IRC, or the APB peripheral clock

Clock Sources



LPC2300/2400 series members

Part Number	Flash (KB)	RAM (KB)	Ethernet	USB (Device/ Host /OTG)	CAN	LCD Controller	External Memory Interface	Pins
LPC2478	512	98	Yes	D/H/O	2	Yes	32-bit	208
LPC2470	0	98	Yes	D/H/O	2	Yes	32-bit	208
LPC2468	512	98	Yes	D/H/O	2	No	32-bit	208
LPC2460	0	98	Yes	D/H/O	2	No	32-bit	208
LPC2458	512	98	Yes	D/H/O	2	No	16-bit	180
LPC2420	0	82	No	D/H/O	0	No	32-bit	208
LPC2388	512	98	Yes	D/H/O	2	No	8-bit	144
LPC2387	512	98	Yes	D	2	No	No	100
LPC2378	512	58	Yes	D	2	No	8-bit	144
LPC2377	512	58	Yes	No	0	No	8-bit	144
LPC2368	512	58	Yes	D	2	No	No	100
LPC2367	512	58	Yes	No	0	No	No	100
LPC2366	256	58	Yes	D	2	No	No	100
LPC2365	256	58	Yes	No	0	No	No	100
LPC2364	128	34	Yes	D	2	No	No	100
LPC2362	128	58	Yes	D/H/O	2	No	No	100
LPC2361	64	34	No	D/H/O	2	No	No	100

